2121
PATENT #2 BJ
4-26-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: : Atty. Docket No.: 00-LM-134
William A. CHREN, Jr. : Group Art Unit: 2121
Serial No.: 10/033,992 : Confirmation No.: 9153
Filed: December 27, 2001 :
For: SELF-TIMED DIGITAL PROCESSING CIRCUITS :



## INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D. C. 20231

Sir:

The attached Form PTO-1449 provides a listing of information which may be relevant to the subject application. This IDS is not intended as a representation that better art is not available, nor that the information provided is prior art.

This IDS is submitted under:
__XX__ 37 CFR 1.97(b) - No Fee.
____ 37 CFR 1.97(c) - No Fee, with Certification.
____ 37 CFR 1.97(c) - Fee.
____ 37 CFR 1.97(d) - Fee, Certification & Petition.

The Commissioner is authorized to charge any required fees under 37 CFR 1.17(p) and (i) (1) to Deposit Account No. **50-1556.**

Respectfully submitted,

Date: 4/15/02

By: _____
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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service by first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231

Kathleen Smith — Name of Person Mailing Paper
Kathleen Smith — Signature of Person Mailing Paper
4/15/02 — Date of Deposit

| Form PTO-1449 U.S. Dept. of Commerce Patent & Trademark Office<br>List of Documents Cit d by Applicant<br>(Use several sheets if necessary) | Atty. Docket: 00-LM-134 | Serial No. 10/033,992 |
|---|---|---|
| | Applicant: William A. CHREN, Jr | |
| | Filing Date: December 27, 2001 | Group: 2121 |



## U.S. PATENT DOCUMENTS

| Ex'rs In'l | | Document Number | Date | Name | Class | Sub-class | Filing Date, if applicable |
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| | AA2 | 09/383,478 | | | | | August 26, 1999 |
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| | | Document Number | Date | Country | Class | Sub-class | Transl'n Yes/No |
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| | AA5 | Karim Arabi et al., "Oscillation Built-In Self-Test (OBIST) Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits", Proceedings of the IEEE International Test Conference, Washington, D.C., 1997, pp. 786-795. |
| | AA6 | N. S. Szabo, et al., "Residue Arithmetic and its Applications to Computer Technology, McGraw-Hill, 1967, pgs. 147-150. |
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| Examiner: | Date Considered: |
|---|---|

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.